

What Is Claimed Is:

1 1. A method for achieving low gate leakage current in an integrated
2 circuit during sleep mode, comprising reducing a power supply voltage applied to
3 the integrated circuit to a low voltage level upon entering sleep mode, wherein the
4 low voltage level is low enough to achieve low gate leakage current, but is high
5 enough to maintain state in the integrated circuit.

1 2. The method of claim 1, wherein the low voltage level is so low that
2 the integrated circuit cannot perform computation operations on data.

1 3. The method of claim 1, wherein the low voltage level is below a
2 threshold voltage for transistors on the integrated circuit.

1 4. The method of claim 1, further comprising restoring the power
2 supply voltage to a nominal operating voltage upon detecting that sleep mode is
3 about to be exited.

1 5. The method of claim 4, wherein reducing the power supply voltage
2 involves gradually ramping the power supply voltage to the low voltage level to
3 reduce noise caused by the voltage change.

1 6. The method of claim 4, wherein restoring the power supply voltage
2 involves gradually ramping the power supply voltage to the nominal operating
3 voltage to reduce noise caused by the voltage change.

1 7. The method of claim 4, wherein reducing the power supply voltage
2 involves stepping the power supply voltage in discrete steps to the low voltage
3 level to reduce noise caused by the voltage change.

1 8. The method of claim 4, wherein restoring the power supply voltage
2 involves stepping the power supply voltage in discrete steps to the nominal
3 operating voltage to reduce noise caused by the voltage change.

1 9. The method of claim 1, wherein the low voltage level is also low
2 enough to provide a low subthreshold leakage current in the integrated circuit.

1 10. An apparatus for achieving low gate leakage current in an
2 integrated circuit during sleep mode, comprising a reducing mechanism
3 configured to reduce a power supply voltage applied to the integrated circuit to a
4 low voltage level upon entering sleep mode, wherein the low voltage level is low
5 enough to achieve low gate leakage current, but is high enough to maintain state
6 in the integrated circuit.

1 11. The apparatus of claim 10, wherein the low voltage level is so low
2 that the integrated circuit cannot perform computation operations on data.

1 12. The apparatus of claim 10, wherein the low voltage level is below
2 a threshold voltage for transistors on the integrated circuit.

1 13. The apparatus of claim 10, further comprising a restoring
2 mechanism configured to restore the power supply voltage to a nominal operating
3 voltage upon detecting that sleep mode is about to be exited.

1 14. The apparatus of claim 13, wherein reducing the power supply
2 voltage involves gradually ramping the power supply voltage to the low voltage
3 level to reduce noise caused by the voltage change.

1 15. The apparatus of claim 13, wherein restoring the power supply
2 voltage involves gradually ramping the power supply voltage to the nominal
3 operating voltage to reduce noise caused by the voltage change.

1 16. The apparatus of claim 13, wherein reducing the power supply
2 voltage involves stepping the power supply voltage in discrete steps to the low
3 voltage level to reduce noise caused by the voltage change.

1 17. The apparatus of claim 13, wherein restoring the power supply
2 voltage involves stepping the power supply voltage in discrete steps to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 18. The apparatus of claim 10, wherein the low voltage level is also
2 low enough to provide a low subthreshold leakage current in the integrated circuit.

1 19. An integrated circuit that achieves low gate leakage current during
2 sleep mode, comprising a reducing mechanism configured to reduce a power
3 supply voltage applied to the integrated circuit to a low voltage level upon
4 entering sleep mode, wherein the low voltage level is low enough to achieve low
5 gate leakage current, but is high enough to maintain state in the integrated circuit.

1 20. The integrated circuit of claim 19, wherein the low voltage level is
2 so low that the integrated circuit cannot perform computation operations on data.

1 21. The integrated circuit of claim 19, wherein the low voltage level is
2 below a threshold voltage for transistors on the integrated circuit.

1 22. The integrated circuit of claim 19, further comprising a restoring
2 mechanism configured to restore the power supply voltage to a nominal operating
3 voltage upon detecting that sleep mode is about to be exited.

1 23. The integrated circuit of claim 22, wherein reducing the power
2 supply voltage involves gradually ramping the power supply voltage to the low
3 voltage level to reduce noise caused by the voltage change.

1 24. The integrated circuit of claim 22, wherein restoring the power
2 supply voltage involves gradually ramping the power supply voltage to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 25. The integrated circuit of claim 22, wherein reducing the power
2 supply voltage involves stepping the power supply voltage in discrete steps to the
3 low voltage level to reduce noise caused by the voltage change.

1 26. The integrated circuit of claim 22, wherein restoring the power
2 supply voltage involves stepping the power supply voltage in discrete steps to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 27. The integrated circuit of claim 19, wherein the low voltage level is
2 also low enough to provide a low subthreshold leakage current in the integrated
3 circuit.
